WHAT IS CLAIMED IS:

1. A receiver apparatus having a demodulator circuit that demodulates transmitted serial data into parallel data by sampling the transmitted serial data on the basis of first and second clock signals having different numbers of clocks to be output in synchronization with a cycle of a transmitted clock, said receiver apparatus comprising:

a first synchronizing circuit generating the first clock signal synchronized with the cycle of the transmitted clock; and

a second synchronizing circuit generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal,

wherein the demodulator circuit comprises the second synchronizing circuit, a sampling register storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference between the transmitted serial data and the input clock signal on the basis of the sampled data, and a clock select circuit that adjusts a phase of a symbol-sampled signal on the basis of the difference.

2. A receiver apparatus having at least two demodulator circuits that demodulate transmitted serial data into parallel data by sampling the transmitted serial data on the basis of first and second clock signals having different numbers of clocks to be output in synchronization with a cycle of a transmitted clock, said receiver apparatus comprising:

a first synchronizing circuit generating the first clock signal synchronized with the cycle of the transmitted clock; and

a plurality of second synchronizing circuits generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal;

wherein:

each of said at least two demodulator circuits comprises any one of said plurality of second synchronizing circuits, a sampling register storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference between the transmitted serial data and the input clock signal on the basis of a sampled data, and a clock select circuit that adjusts a phase of a symbol-sampled signal on the basis of the difference; and

a lowpass filter circuit included in one of said at least two modulator circuits is shared by another modulator circuit as the lowpass filter.

3. The receiver apparatus as claimed in claim 1, wherein at least two said second synchronizing circuits share a phase detection circuit.

4. The receiver apparatus as claimed in claim 1, wherein the first synchronizing circuit inputs the first clock signal into at least two said synchronizing circuits.

5. The receiver apparatus as claimed in claim 1, further comprising a voltage control oscillator that generates the second clock signal on the basis of a controlled voltage output from the lowpass filter circuit.

6. The receiver apparatus as claimed in claim 1,

further comprising a voltage control delay circuit that generates the second clock signal on the basis of a controlled voltage output from the lowpass filter circuit.

7. The receiver apparatus as claimed in claim 1, further comprising a phase locked loop circuit or a delay locked loop circuit that includes the lowpass filter to be shared.

8. The receiver apparatus as claimed in claim 1, wherein the first synchronizing circuit includes a phase locked loop circuit, and the second synchronizing circuit includes a delay locked loop circuit having the lowpass filter to be shared.

9. The receiver apparatus as claimed in claim 1, wherein the second synchronizing circuit generates the second clock signal having an n number of phases that satisfies $n/m - 1 < 1/3$, where the first clock signal has the n number of phases and the second clock signal has an m number of phases.

10. The receiver apparatus as claimed in claim 1, wherein the second synchronizing circuit generates the second clock signal having an m number of phases that satisfies $m/n - 1 < 1/3$, where the first clock signal has an n number of phases and the second clock signal has the m number of phases.

11. The receiver apparatus as claimed in claim 1, wherein the clock select circuit selects multiple clocks synchronized with the transmitted clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference calculating circuit in order to adjust a phase relation of the transmitted clock in

synchronization with the cycle of the transmitted clock.

12. The receiver apparatus as claimed in claim 1, further comprising a quality evaluation circuit that evaluates a quality value of the transmitted serial data on the basis of the sampling data.

13. A receiver apparatus comprising:

a first synchronizing circuit generating a first clock signal synchronized with a cycle of a transmitted clock; and

a plurality of demodulator circuits,

wherein:

each of said plurality of demodulator circuits includes a second synchronizing circuit generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal, a sampling register storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit that selects multiple clocks synchronized with the transmission clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference calculating circuit in order to adjust a phase relation of the transmission clock while synchronized with the cycle of the transmitted clock; and

at least one of the second synchronizing circuit included in each of said plurality of demodulator circuits generates the second clock signal on the basis of a controlled voltage output from a lowpass filter

circuit included in the second synchronizing circuit in another demodulator circuit.

14. A receiver apparatus comprising:

a first synchronizing circuit generating a first clock signal synchronized with a cycle of a transmitted clock; and

a plurality of demodulator circuits,

wherein:

each of said plurality of demodulator circuits includes a second synchronizing circuit generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal, a sampling register storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit that selects multiple clocks synchronized with the transmission clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference calculating circuit in order to adjust a phase relation of the transmission clock while the second synchronizing circuit is being synchronized with the cycle of the transmitted clock; and

at least one of the second synchronizing circuit included in each of said plurality of demodulator circuits includes a lowpass filter circuit, supplies an output from the lowpass filter circuit to another demodulator circuit, and generates the second clock signal on the basis of a controlled voltage output from the lowpass filter circuit included in the second synchronizing circuit in another demodulator circuit.

15. A receiver apparatus comprising:

a first synchronizing circuit generating a first clock signal synchronized with a cycle of a transmitted clock;

a controlled voltage output circuit that outputs a controlled voltage to generate a second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal; and

a demodulator circuit that includes a second synchronizing circuit that generates a second clock signal on the basis of the controlled voltage output from the controlled voltage output circuit, a sampling register storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit selects multiple clocks synchronized with the transmitted clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the controlled voltage output circuit in order to adjust a phase relation of the transmitted clock while synchronized with the cycle of the transmitted clock.